Enrollment No: _____ Exam Seat No:_____

C.U.SHAH UNIVERSITY

Summer Examination-2018

Subject Name : Advanced Computer Architecture

Subject Code : 4TE08ACA1 Branch: B.Tech (IT)

Semester : 8 Date : 24/04/2018 Time : 02:30 To 5:30 Marks : 70

Instructions:

(1) Use of Programmable calculator & any other electronic instrument is prohibited.
(2) Instructions written on main answer book are strictly to be obeyed.
(3) Draw neat diagrams and figures (if necessary) at right places.
(4) Assume suitable data if needed.

Q-1 **Attempt the following questions:** **(14)**

a) What is virtual memory? (1)

b) Which are stages for Instruction pipelining? (1)

c) Define: Computer Architecture. (1)

d) What is multi-core processor? (1)

e) What is IPL? (1)

f) _____is a term used to denote a large class of techniques that are used to provide simultaneous data processing tasks. (1)
(A). Shared memory (B). Parallel processing (C). Memory hierarchy (D). None

g) _____represents an organization that includes many processing units under the supervision of a common control unit. (1)
(A). SISD (B).SIMD (C). MIMD (D). MISD.

h) RAID is_____. (1)
(A). Input Device (B). Storage Device (C). Output Device. (D) None of Above

i) Write through and write back are two strategies for maintaining: (1)
(A). Locality of reference (B). Collision (C). Coherence (D). All of above

j) TLB is used in: (1)
(A). Paging (B). Segmentation (C). Both A&&B (D). None of above

k) A multiprocessor system with common shared memory is called: (1)
(A). Loosely coupled system (B). Tightly coupled system (C). Both a and b
(D) None of Above

l) In paging, if demanded page is not found it is declared is: (1)
(A). Page miss (B). Page fault (C). Page empty (D). Both A and C

m) Which of not an address mapping scheme: (1)
(A). Direct mapping (B). Associate mapping (C). Direct Associate Mapping
(D). Set Associate Mapping

n) Vector processing is not part of : (1)
(A). Parallel Processing (B). Multiprocessing (C). Batch mode processing
(D). Array processing

Attempt any four questions from Q-2 to Q-8

Q-2		**Attempt all questions**	**(14)**
	(a).	Briefly discuss various levels of RAID.	**(7)**
	(b).	What is Reservation table? Explain it with linear and none-linear pipeline processor.	**(7)**
Q-3		**Attempt all questions**	**(14)**
	(a).	Write a technical note on compiler optimization to reduce the miss rate.	**(7)**
	(b).	Explain in detail the SMT architecture and its challenges**.**	**(7)**
Q-4		**Attempt all questions**	**(14)**
	(a).	Explain Arithmetic pipeline design.	**(7)**
	(b).	Explain Basic structure of a centralized shared-memory and distributed multiprocessor.	**(7)**
Q-5		**Attempt all questions**	**(14)**
	(a).	Explain Instruction pipeline design.	**(5)**
	(b).	Explain paging, segmentation and TLB.	**(5)**
	(c).	Explain inclusion, coherence and locality of references.	**(4)**
Q-6		**Attempt all questions**	**(14)**
	(a).	Write a note on Data Hazard.	**(5)**
	(b).	Explain Hierarchical Memory Technology.	**(5)**
	(c).	Define following terms: speedup, efficiency, throughput and pipeline stalling.	**(4)**
Q-7		**Attempt all questions**	**(14)**
	(a).	Describe the implementation of directory-based cache coherence protocol.	**(7)**
	(b).	Discuss various steps to be followed in designing I/O system.	**(7)**
Q-8		**Attempt all questions**	**(14)**
	(a).	Differentiate between multithreading computers and multi processor systems.	**(5)**
	(b).	Explain page replacement policies.	**(5)**
	(c).	Explain symbolic processor.	**(4)**